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Performance and EMI Assessment of Post-800V Traction Inverter Topologies for EV Applications

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Executive Summary

The shift to post-800V electric vehicle (EV) architectures offers key advantages, including shorter charging times, lower charging currents, and reduced system weight (due to smaller conductor cross-sections), all of which enhance overall vehicle performance. However, identifying suitable traction inverter topologies that meet automotive requirements for efficiency, electromagnetic interference (EMI), and reliability remains critical. Hence, this study presents a comparative analysis of traction inverter topologies, especially 2-Level H-Bridge, 3-Level T-Type, and 3-Level Active Neutral-Point Clamped (ANPC) as a potential candidate for post-800V applications. Virtual verifications via simulations have been conducted on several DC-link voltages of 800V, 1000V, and 1200V, and the power losses, junction temperature, efficiency, and electromagnetic interference (EMI) are compared. The results have demonstrated that multilevel inverters can significantly reduce switching losses, reduce mean junction temperature, and exhibit superior EMI performance due to their lower voltage steps and more favorable current conduction paths. These findings support optimizing the design and layout of the post-800V traction inverter.

Keywords: Electric Vehicle, Drive & Propulsion Systems, Wide Bandgap Devices & Related Issues, Power Electronics Systems, Thermal Management, Electromagnetic Compatibility.

1 Introduction

Recent advancements in electric vehicle (EV) technologies have intensified the push toward higher voltage powertrain architectures. While conventional EVs operated with 400 V battery systems, the demand for faster charging, higher efficiency, and improved range has driven the transition toward higher battery voltage levels, notably beyond 800 V [1], [2]. Increasing the battery voltage reduces the current required for a given power output, directly lowering resistive losses (I^2R) in the cables and connectors, minimizing heating, and enabling the use of lighter and thinner conductors [3]. These improvements not only enhance overall powertrain efficiency but also contribute to weight reduction, supporting better vehicle performance and extended driving range. Although higher voltages could, in theory, continue to bring additional benefits, practical challenges emerge beyond certain thresholds. Moving to voltages beyond 800V would impose stringent insulation requirements, increase the risk of partial discharge, and demand components capable of

withstanding much higher breakdown voltages and higher voltage peaks dv/dt [4], [5]. High-voltage-rated components, such as switches, connectors, and capacitors, generally involve larger physical sizes, stricter clearance and creepage distances, and higher materials costs [6]. Additionally, today's public ultra-fast charging networks, while evolving, are predominantly designed to accommodate up to 800 V systems, as seen in models like the Porsche Taycan, Hyundai IONIQ 6, and Lucid Air [7]. Though there are emerging chargers supporting 900–1000 V levels, widespread support for ultra-high voltages remains limited [8]. Leading this trend, manufacturers like BYD have introduced 1000V architectures, setting new benchmarks for charging speed and range in next-generation EV platforms (5 minutes of charging for 400 kilometers of range) [9]. Thus, operating within the 800 V to approximately 1000–1200 V range offers a practical trade-off between improved system performance and manageable cost, insulation, and infrastructure compatibility.

In EV systems, the traction inverter becomes critical, acting as the interface between the battery and the motor. The inverter must efficiently manage large DC-link voltages while minimizing switching losses, conduction losses, electromagnetic interference (EMI), and thermal stress. Two-level (2L) inverters, widely used traction inverter topology, switch directly between the positive and negative rails of the DC link, subjecting the system to large voltage steps during every switching event [10]. These large voltage transitions (high dv/dt) can excite parasitic capacitances between the inverter, motor, and chassis, leading to elevated common-mode (CM) and differential-mode (DM) EMI emissions. Additionally, the sharp voltage edges stress motor insulation and increase the risk of partial discharge, especially in higher-voltage systems [11].

To mitigate these challenges, even at higher DC-link voltage (i.e., post 800 V), alternative inverter topologies have been investigated for EV applications. Among these, three-level (3L) configurations, including the Active Neutral Point Clamped (ANPC) and T-Type topologies, are considered as potential candidates due to their ability to split the DC-link voltage into smaller switching steps [12]. By limiting the instantaneous voltage changes across the switches and the motor terminals, these topologies reduce dv/dt, lower EMI, and improve output waveform quality. Moreover, distributing voltage stress across multiple devices can enhance reliability and reduce the demands placed on individual components. Besides, multi-level inverter topologies reduce current ripple effect, the reduction of current ripple allows for a more straightforward motor design. Silicon carbide (SiC) power devices have been instrumental in enabling these advances. SiC devices offer superior characteristics compared to traditional silicon IGBTs, including lower conduction losses, higher switching speeds, higher breakdown voltages, and better thermal performance [13]. However, the faster switching transitions inherent to SiC devices result in sharper dv/dt slopes, which, if not carefully managed through inverter design, can worsen high-frequency EMI emissions compared to silicon-based counterparts.

Although considerable research has been conducted on improving individual aspects, such as inverter efficiency, thermal management, or EMI suppression, there remains a lack of studies comparing different inverter topologies for post-800 V operating conditions. In particular, systematic evaluations that consider efficiency, switching and conduction losses, junction temperature behavior, EMI emissions, and cost simultaneously under realistic thermal constraints are still limited [14], [15].

This research aims to address these gaps by comparatively analyzing three inverter topologies—2L H-Bridge, 3L ANPC, and 3L T-Type—for high-voltage EV traction applications. Using detailed electro-thermal and EMI-focused simulations with discrete SiC MOSFETs (C2M0045170P and E4M0013120K from Wolfspeed), the study evaluates performance at input voltages of 800 V, 1000 V, and 1200 V. Simulations are conducted under air natural (AN) cooling conditions to reflect practical thermal management limitations. Key metrics such as conduction and switching losses, junction temperature variation, EMI characteristics (common-mode and differential-mode), overall efficiency, and active component cost are analyzed.

2 Comparison of existing topologies

This paper focuses on the evaluation of three specific inverter topologies illustrated in Figure 1: the 2L-H-Bridge, the 3L-ANPC, and the 3L-T-Type. Although alternative and more complex Multi-Level Inverter (MLI) configurations, such as the Split Inductor MLI, Flying Capacitor MLI, and Cascade H-Bridge, are available, the selected topologies remain the most competitive for the automotive applications. The 2L-H-Bridge (Figure 1(a)) is the most widely used and straightforward topology in EV industries, consisting of six switches. Each switch has a blocking voltage equal to the DC-bus voltage (Vdc). In the figure, the switches that are subjected to a blocking voltage equal to the input DC-bus voltage (Vdc) are highlighted in light orange, while those facing half the DC-bus voltage (Vdc/2) are marked with a light green-shaded rectangle.

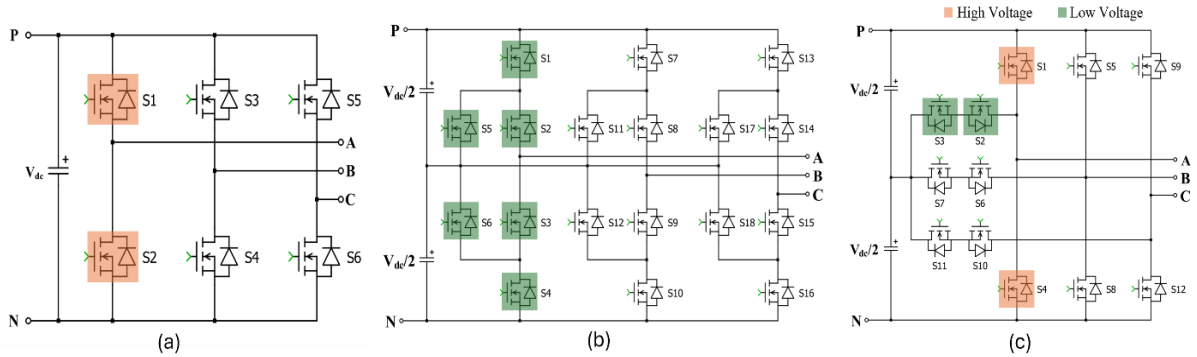

Figure 1: Three-phase inverter topologies: (a) 2L H-Bridge, (b) 3L ANPC, (c) 3L T-Type.

While this topology is cost-effective due to its simplicity, one of its primary drawbacks is the increase in switching losses at higher switching frequencies, which negatively impacts overall efficiency.

The 3L Active Neutral Point Clamped (ANPC) inverter (Figure 1(b)) offers significant advantages in terms of reducing switching losses. In this topology, two series-connected switches in each leg share the blocking voltage, meaning each switch experiences only half of the DC-bus voltage (Vdc/2). This voltage division reduces the cumulative switching losses because the combined switching loss of two switches blocking Vdc/2 is lower than that of a single switch blocking the full Vdc. As a result, the switching frequency of the 3L ANPC inverter can be increased without significantly compromising efficiency. This makes the 3L ANPC inverter an attractive option for applications requiring higher switching frequencies and improved efficiency, despite the slightly more complex design compared to the 2L-H-Bridge.

The 3L T-Type inverter (Figure 1(c)) resembles the traditional 2L-H-Bridge, with a bidirectional switch linked between the switching power-pole and the midpoint of Vdc '0,' so creating a T-configuration. The bidirectional switch is often constructed using two common-drain or common-source MOSFET switches. The clamping mechanism of the T-Type differs from that of the ANPC. The inverter leg may be constructed utilizing devices with varying voltage ratings. The upper and lower switches, S1 and S2, must possess a blocking voltage of Vdc, in contrast to Vdc=1/2 for the bidirectional switch. The conduction losses of the T-Type inverter are lower than those of the ANPC topology, as there are no two series-connected switches in each inverter leg. As a result, the 3L T-Type inverter is often regarded as a hybrid solution that combines the benefits of both the 2L-H-Bridge and the 3L ANPC topologies.

3 Results and analysis

In this paper, the simulation uses SiC semiconductor switches of 1200V (E4M0013120K) and 1700V (C2M0045170P), chosen based on the voltage stress unique to each topology. This tailored approach enables a precise comparison of power losses, junction temperature variations, and overall efficiency across the three inverter topologies. In the 2L H-Bridge and the upper and lower switches of the 3L T-Type inverter, 1700V-rated switches are used, as these components experience the full DC-bus voltage. For the 3L ANPC and the 'T' branch of the 3L T-Type inverter, 1200V-rated switches are utilized since these switches handle only half of the DC-bus voltage.

All simulations have been carried out using an identical total simulation time to ensure a uniform basis for comparison. Maintaining a fixed simulation duration ensures that transient effects and thermal stabilization are treated equally across all cases. Furthermore, all topologies have been evaluated under the same operating point, with a constant output current, load, and unified modulation scheme. This eliminates discrepancies that could arise from unequal loading or differing dynamic conditions, allowing the analysis to isolate the intrinsic performance of each inverter architecture. By keeping the current constant across simulations, the influence of input voltage on electromagnetic interference (EMI), switching behavior, and thermal loading can be fairly assessed. The results shown in this section—covering conduction and switching losses, junction temperature change, inverter efficiency, and EMI characteristics—are thus directly comparable and reflect only the topological and voltage-based differences inherent to each design. This methodological consistency ensures that the conclusions drawn are rooted in physical behavior, not simulation setup artifacts.

3.1 Power loss and efficiency for different input voltages

Figure 2 provides a comprehensive evaluation of power loss comparison and overall inverter efficiency of the power stage for the 2L H-Bridge, 3L ANPC, and 3L T-Type topologies at three distinct input voltage levels: 800 V, 1000 V, and 1200 V, only considering losses of power semiconductor device. The comparisons are carried out at a fixed output power of 120 kW under steady-state operating conditions and equal simulation duration. As shown in Figure 2(a), the total power loss decreases significantly with increasing input voltage for all topologies. This trend can be attributed to the reduction in output current at higher DC bus voltages for the same output power, which directly lowers conduction losses—a dominant component in total losses. Among the three topologies, the 3L ANPC consistently demonstrates the highest total power loss, followed by the 3L T-Type and the 2L H-Bridge. The increased loss in the ANPC occurs from its more complex conduction path, which involves a greater number of active switches and clamping diodes.

The conduction loss trends are further detailed in Figure 2(b). These losses scale with the square of the phase current and the cumulative on-state resistance in the conduction path. The ANPC topology exhibits the highest conduction losses across all voltages due to the involvement of multiple series-connected switches and diodes in each current path, which increases the equivalent $R_{DS(on)}$. Conversely, the 2L H-Bridge achieves the lowest conduction losses, benefiting from a simplified conduction path with only two switches per phase. The 3L T-Type topology provides a balance, exhibiting lower conduction loss than the ANPC due to its more optimized current path and reduced cumulative resistance.

The switching loss behavior is illustrated in Figure 2(c). Notably, switching losses remain relatively constant across different input voltages within each topology. This is expected since the switching frequency and the energy loss per transition remain largely unaffected by the input voltage under fixed output power conditions. However, when comparing across topologies, the 2L H-Bridge encounters the highest switching loss, which is more than double that of the ANPC and T-Type. This is because each device in the 2L inverter switches the full DC-link voltage and the full load current during each commutation, leading to significantly higher energy dissipation per switching event. In contrast, 3L topologies distribute switching transitions among multiple devices, often at partial voltages and reduced current stress, particularly the clamping switch in the T-Type, which operates under reduced electrical stress and switches at a lower rate, thereby minimizing overall switching loss.

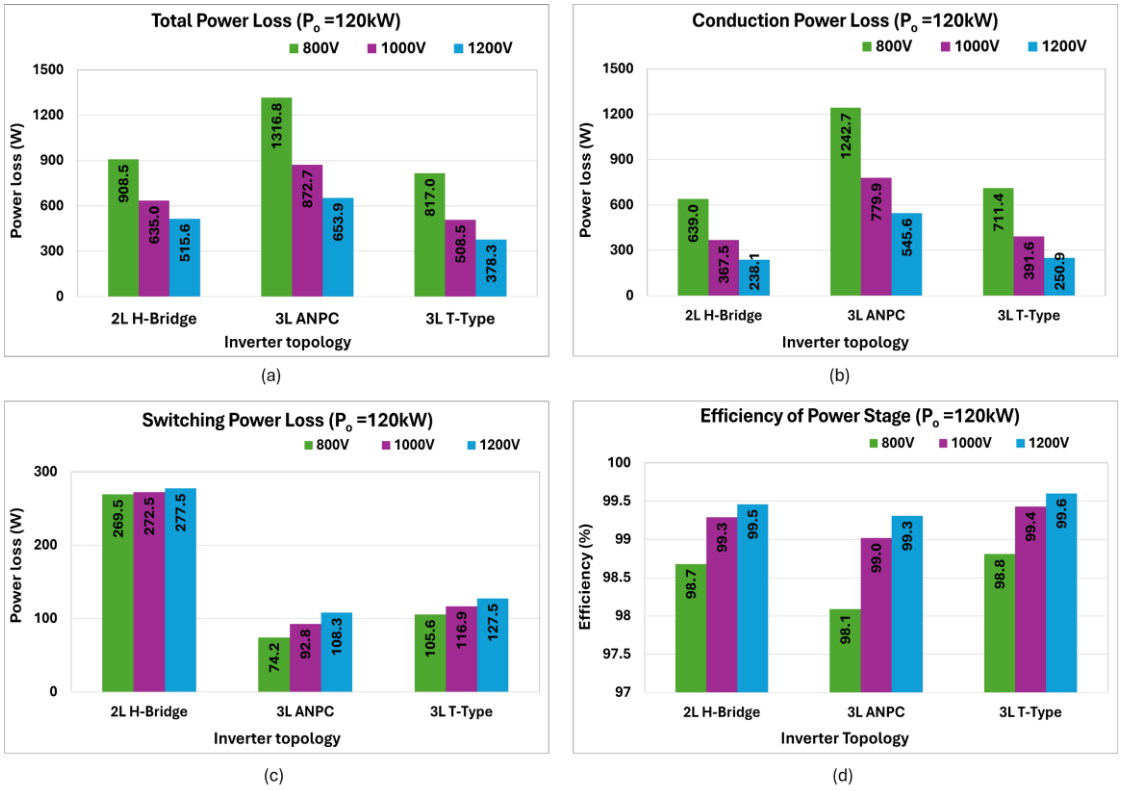

Figure 2: Power loss and efficiency for different input voltages at a fixed output power.

Figure 2(d) summarizes the overall power stage efficiency as a function of input voltage. A clear upward trend is observed for all topologies as voltage increases from 800 V to 1200 V. Among the topologies, the 3L T-Type achieves the highest efficiency across all tested voltage levels, reaching 99.6% at 1200 V. This superior performance results from its combined advantages of moderate switching loss and significantly reduced conduction loss, especially when compared to the 3L ANPC. While the 2L H-Bridge benefits from low conduction loss, its elevated switching loss ultimately limits its peak efficiency. Meanwhile, the 3L ANPC suffers from high conduction losses, despite maintaining switching loss levels similar to the T-Type, which constrains its overall efficiency.

In short, this analysis highlights that the 3L T-Type inverter delivers the most favorable electrothermal and efficiency performance for post-800V traction applications, making it a strong candidate for future high-voltage electric drivetrain designs.

3.2 Power loss and junction temperature variations

In this paper, for thermal analysis, the junction temperature (T_j) of the upper switch in each inverter leg is considered for three topologies and all evaluated under air natural (AN) cooling, 25°C of ambient temperature at a fixed output power of 120 kW. The upper and lower switches (S1 and S2 in the 2L H-Bridge, S1 and S4 in the 3L ANPC and T-Type), which experience the highest electrical stress, are considered thermally critical. These devices handle substantial DC-link voltage and load current, making them key indicators of each topology's thermal behavior. As shown in Figure 3, the 2L H-Bridge exhibits the highest junction temperatures, reaching 93.5 °C at 800 V, decreasing to 65.9 °C at 1200 V. This trend results from its simple architecture, where just two active switches conduct full DC-link voltage and total phase current without any sharing. This places a heavy thermal load on a limited number of devices, leading to increased junction temperatures. Without additional cooling, this design may require larger heatsinks or even forced-air cooling, ultimately reducing the power density of the system, an important factor in electric vehicle (EV) design. In contrast, both 3L topologies maintain significantly lower junction temperatures across all voltage levels. Their architectures allow current conduction and switching transitions to be shared among more devices, reducing thermal stress on any individual switch. The 3L ANPC, for instance, uses a more complex conduction path that includes multiple active switches and clamping devices, allowing thermal energy to be distributed more evenly. Even though the ANPC shows higher total power loss (as seen in Figure 2a) compared to the others, the upper switch only reaches 62.0 °C at 800 V, which indicates that this ANPC topology offers better thermal performance.

The 3L T-Type inverter demonstrates the best thermal performance among the evaluated topologies, with the upper switch reaching a junction temperature of just 43.2 °C at 1200 V. This advantage is primarily attributed to its balanced current conduction and loss distribution strategy. While the high-side switch (S1) is subjected to the full DC-link voltage, the clamping switches (S2 and S3) operate under significantly reduced voltage and current stress. Their involvement in handling transitions under milder electrical conditions results in minimal conduction and switching losses. This effective distribution of thermal load across multiple devices helps reduce localized heating and peak power dissipation. As a result, the T-Type inverter maintains a more uniform and lower junction temperature profile, even when operating under natural air (AN) cooling, making it thermally superior for high-voltage EV applications.

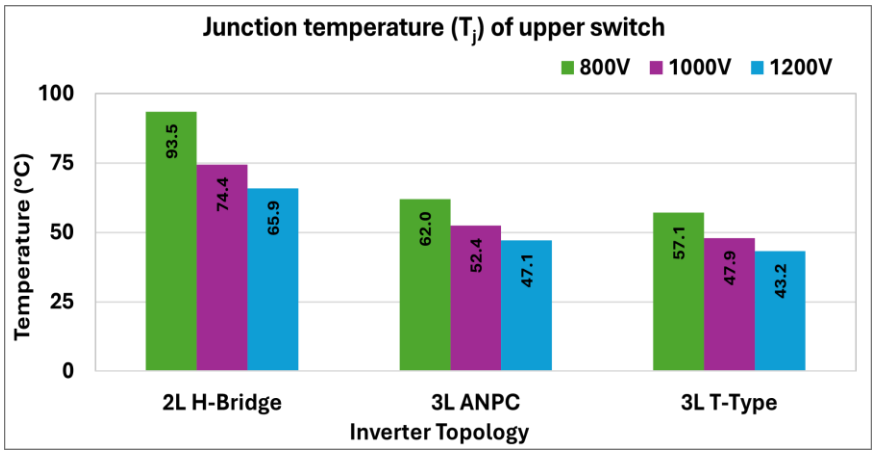

Figure 3: Junction temperature of the upper switch for different input voltages.

Figure 4 presents a dynamic performance assessment of the three inverter topologies by analyzing how total power loss and junction temperature of the upper switch evolve across a wide output power range (60 kW to 120 kW) under different input voltage levels (800 V, 1000 V, and 1200 V). This transient evaluation offers deeper insight into each topology's thermal performance under varying load conditions, a critical factor in real-world EV drive cycles. Across all three voltage levels, total power loss (left column of subplots a-1, b-1, c-1) increases monotonically with output power for each topology. However, the rate of increase and overall magnitude vary significantly, revealing the sensitivity of each architecture to output loading. The 3L ANPC demonstrates the steepest slope and highest loss accumulation, highlighting its relatively poor scalability in high-load scenarios. This is a consequence of its complex conduction paths involving more devices, where conduction loss compounds more rapidly with increasing current. In contrast, the 3L T-Type shows a more gradual increase in total power loss, underscoring its superior conduction efficiency and ability to maintain lower loss margins under higher loads. The 2L H-Bridge, although efficient at lower power levels, converges toward the T-Type's loss profile at higher outputs due to rising switching stress under full-voltage commutations.

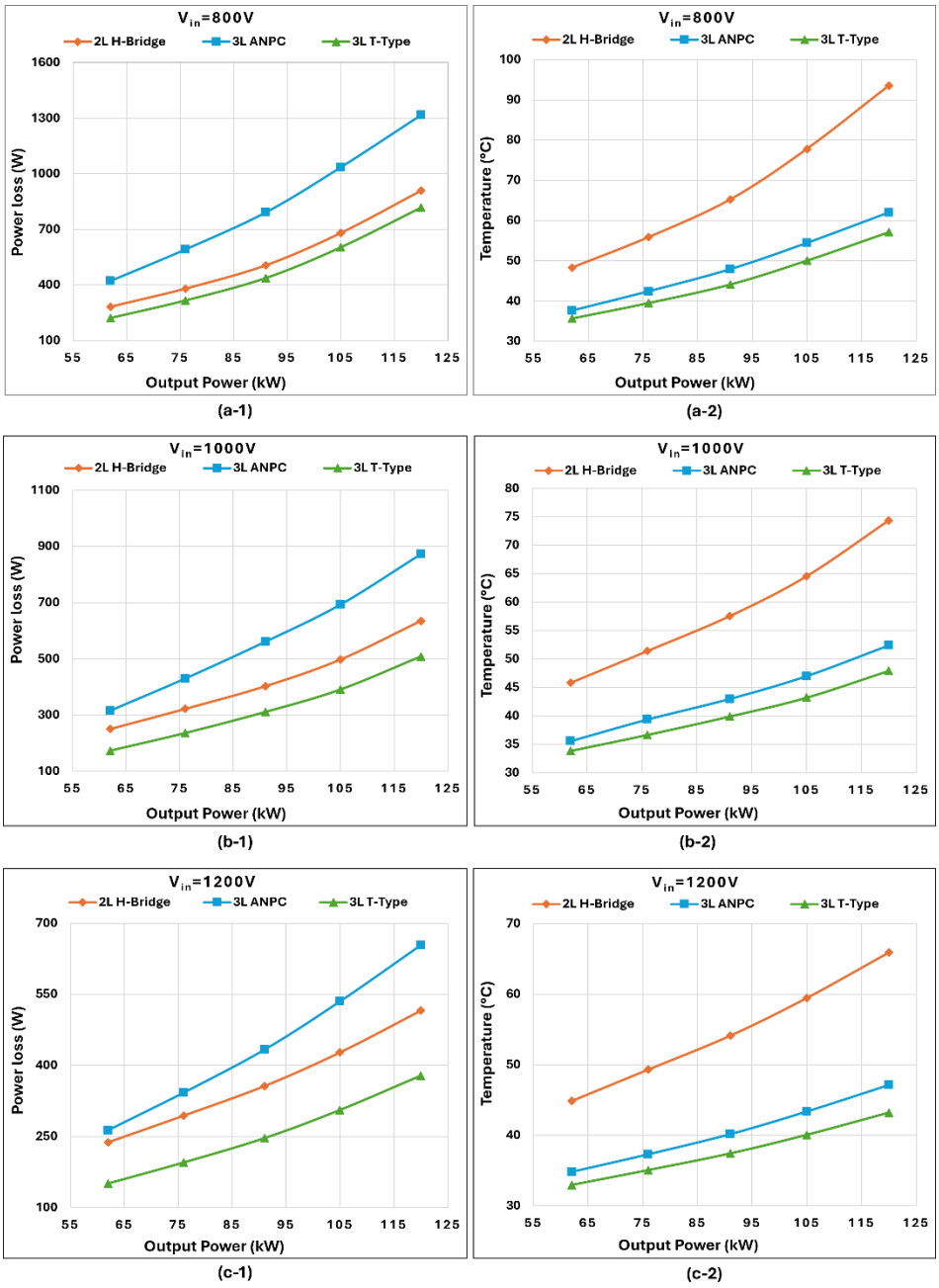

Figure 4: Output power vs. Power loss and junction temperature (a-1&2) 800V, (b-1&2) 1000V, and (c-1&2) 1200V.

The right column of subplots (a-2, b-2, c-2) in Figure 4 depicts the corresponding junction temperature change of the upper switch under the different output power conditions. While the general upward trend is expected due to higher thermal dissipation at elevated power, the thermal gradients across topologies diverge markedly. The 2L H-Bridge exhibits a sharper rise in junction temperature, with the slope increasing more rapidly at higher output powers. This behavior reflects the thermal concentration on fewer switching devices and the lack of current-sharing paths in the 2L architecture. In contrast, the 3L T-Type maintains a relatively linear and mild temperature increase, demonstrating better thermal scalability and distribution of losses even as power levels rise. The 3L ANPC, while not as thermally efficient as the T-Type, benefits from its multilevel structure, showing improved thermal stability over the 2L topology, particularly at mid- to high-power conditions.

Importantly, this figure reveals that while fixed-power comparisons (as shown in Figure 2 and Figure 3) offer static insights, the variable load behavior in Figure 4 validates the superiority of the 3L T-Type inverter under practical operating conditions. It not only maintains lower total losses but also exhibits smoother thermal growth characteristics, which translates to improved reliability and reduced cooling overhead in dynamic EV drive profiles. These attributes make the 3L T-Type an attractive solution for real-world traction systems where output power frequently fluctuates due to acceleration, gradient, and regenerative braking scenarios.

3.3 Switching loss for different switching frequencies

Figure 5 presents the sensitivity of switching losses to switching frequency for three inverter topologies—2L H-Bridge, 3L ANPC, and 3L T-Type—at an input voltage of 1000 V and fixed output power of 120 kW. This analysis provides valuable insights into how each inverter topology responds to switching frequency scaling, which is a critical design consideration when optimizing inverters for high-performance electric vehicle applications. In high-speed EV traction systems, where motors operate at elevated rotational speeds, maintaining a high switching frequency relative to the motor fundamental frequency is essential to ensure good output waveform quality, reduce harmonic losses, and minimize acoustic noise. Across all switching frequencies (10 kHz to 30 kHz), the 2L H-Bridge consistently incurs the highest switching losses. This is due to its inherent architectural limitation: each switch commutates the full DC-link voltage and the complete output current during every switching event. As switching frequency increases, the energy dissipated per second rises linearly, causing a sharp increase in total switching loss—from 85.6 W at 10 kHz to 272.5 W at 30 kHz. This steep scaling severely impacts thermal performance and necessitates more robust cooling or derating, limiting the 2L topology's suitability for high-frequency operation in demanding EV drives. By contrast, the 3L T-Type and ANPC topologies exhibit significantly improved switching efficiency across the frequency range. In both designs, switching transitions are distributed among multiple devices, and certain switches—particularly the clamping devices—operate under reduced voltage and current stress. This results in lower energy per switching event, enabling both topologies to scale frequency with much more manageable increases in switching loss. Notably, the 3L ANPC shows the most favorable loss progression, rising from only 32.2 W at 10 kHz to 92.8 W at 30 kHz. This moderate slope suggests that the ANPC can accommodate higher switching frequencies with less compromise in thermal overhead.

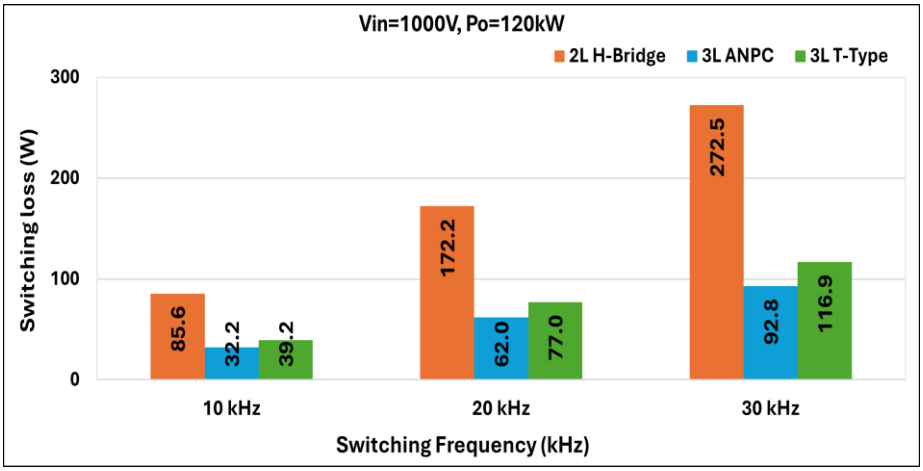

Figure 5: Switching loss at different switching frequencies.

The 3L T-Type inverter, while slightly higher in switching loss compared to the ANPC at each frequency point, maintains a predictable and controlled loss trajectory—from 39.2 W at 10 kHz to 116.9 W at 30 kHz. This performance underscores the T-Type's strong position as a balanced topology that supports both high switching frequencies and manageable thermal output, making it well-suited for high-performance EV applications where switching frequency must be increased to reduce output filter size or improve control bandwidth.

3.4 EMI spectrum for different input voltages

In this study, conducted EMI analysis is analyzed using a standard Line Impedance Stabilization Network (LISN)-based setup implemented in simulation. The LISN consists of a L_{LISN} =5 µH series inductor, decoupling capacitors of 1 µF and 100 nF, and a R_{LISN}50 Ω sensing resistor to capture high-frequency voltage noise at the DC input. To model the parasitic coupling paths from the inverter switching nodes to ground, fixed capacitances are applied across all topologies: 20 pF from the upper switch node to ground, 20 pF from the lower switch node to ground, and 120 pF from the midpoint node to ground. These values are commonly found in EMI literature and represent realistic parasitic paths in high-voltage inverter systems[16]. It is important to note that parasitic capacitances are not standardized, as they depend strongly on physical design parameters such as layout geometry, PCB stackup, package type (e.g., TO-247 vs. surface mount), heatsink grounding, and mounting method. Nevertheless, the selected values provide a consistent baseline and are applied uniformly across all topologies to ensure fair comparative analysis.

In this simulation setup, no EMI filtering components are included. This allows a direct comparison of the inherent EMI performance of each topology without the influence of external suppression networks. Additionally, a fixed load current of 100 A is applied for both 800 V and 1000 V input voltages, and the switching frequency is held constant at 20 kHz, ensuring that EMI results reflect only the impact of topology and input voltage under equal operating stress. Maintaining a constant current ensures that each topology is subjected to equivalent di/dt stress. Meanwhile, as the input voltage changes from 800 V to 1000 V, the applied dv/dt naturally increases. By holding the current constant, the analysis isolates EMI behavior resulting from dv/dt differences alone, ensuring that the influence of switching current is held equal across all test conditions. The EMI spectra presented are based on raw common-mode (CM) and differential-mode (DM) voltage data extracted from the LISN output, providing a clear view of the unfiltered emission characteristics of each inverter configuration.

Figure 6 presents the comparative conducted EMI spectra at input voltages of 800 V and 1000 V. The spectra are derived from time-domain measurements processed through a LISN-based setup, and plotted in terms of common-mode (CM) and differential-mode (DM) interference voltage over a frequency range of 10 kHz to 30 MHz. At both input voltages, a clear distinction in EMI behavior is observed across the topologies. For the 2L H-Bridge, the DM noise dominates across the frequency spectrum, with peak magnitudes nearly 120 dBµV at 1000V input voltage. This is attributed to the large voltage swings and full DC-link transitions per switching event, which inject high-frequency harmonics into the system. The CM noise in the H-Bridge also shows elevated levels, particularly in the low-frequency range driven by strong common-mode voltage pulses due to lack of voltage clamping and minimal common-mode current path decoupling. In contrast, the 3L ANPC and T-Type inverters show markedly improved EMI profiles. For both topologies, the CM and DM spectra remain well below the H-Bridge baseline. This improvement is linked to the multilevel structure, where output voltage transitions occur in smaller steps (e.g., ±Vdc/2 instead of ±Vdc), leading to lower dv/dt and reduced spectral content at high frequencies. Furthermore, the T-Type consistently achieves the lowest EMI among the three, particularly in the CM domain. Its symmetrical switching and use of central clamping switches (operating at reduced stress) help suppress high-frequency noise generation and limit ground-referenced current injection.

The impact of increased input voltage (from 800 V to 1000 V) slightly elevates the overall EMI magnitude, especially in the DM spectrum, due to higher voltage stress and increased switching energy. However, this rise is more pronounced in the 2L topology than in the multilevel counterparts, underlining the inherent EMI mitigation capability of 3L structures. Overall, the results validate that both 3L ANPC and T-Type inverters are superior in EMI behavior, with the T-Type offering the cleanest spectral profile for high-voltage EV inverter applications.

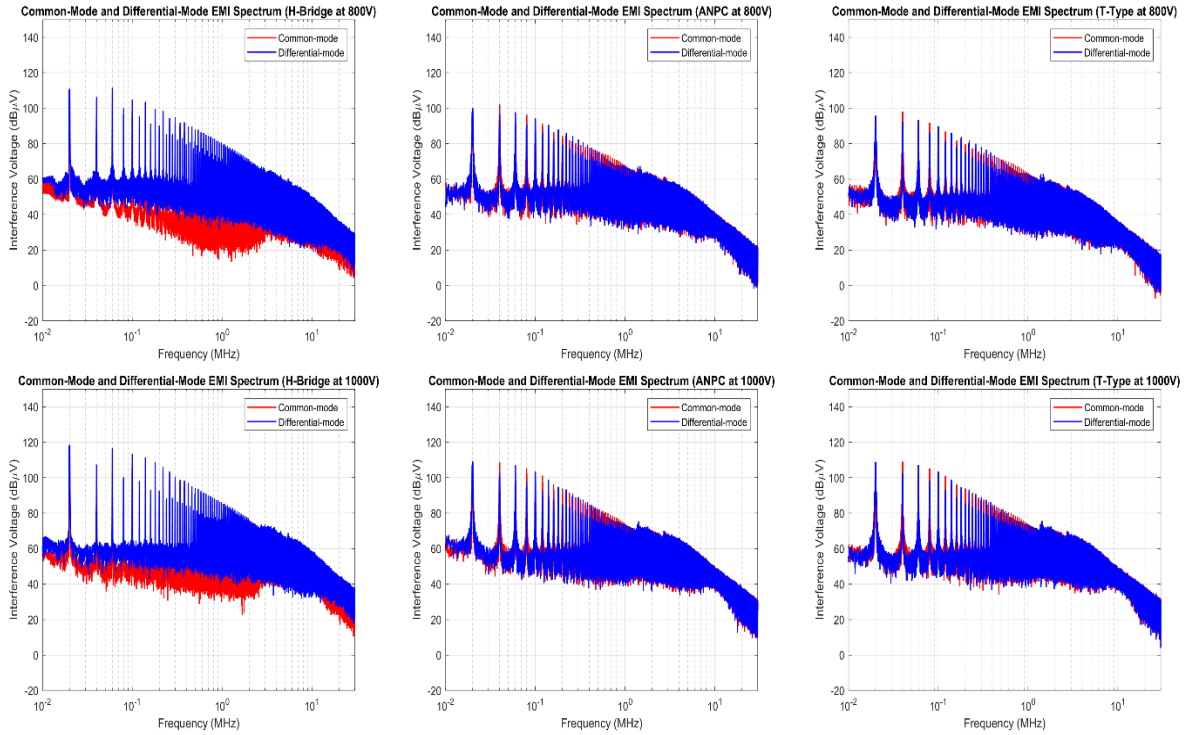

Figure 6: Conducted EMI of different topologies for 800V and 1000V DC link.

4 Cost and Complexity

To provide a practical comparison, Table 1 presents the estimated cost and complexity of each inverter topology based on the number of required power switches and gate drivers. Only power SiC MOSFETs and gate driver components are considered for this estimation, as these elements represent the primary contributors to active component cost in high-voltage EV inverters.

Table 1: Cost and Complexity Comparison of Inverter Topologies

Parameter	2L H-Bridge	3L ANPC	3L T-Type
Total switches (3-phase)	6	18	12
Switch voltage rating	1700 V	1200 V	1700 V (S1/S4), 1200 V (S2/S3)
Paralleling required	Yes (2× per switch)	No	Yes (2× for 1700 V switches)
Total discrete switches	12	18	18
Switch unit price	1700 V = €100	1200 V = €88	1700 V = €100, 1200 V = €88
Total switch cost [17]	12 × €100 = €1,200	18 × €88 = €1,584	(12 × €100) + (6 × €88) = €1,728
Gate drivers required	6	18	12
Gate driver unit price	€45	€45	€45
Total gate driver cost	6 × €45 = €270	18 × €45 = €810	12 × €45 = €540
Total cost (switch + driver)	€1,470	€2,394	€2,268
Cooling requirement	High	Medium-High	Low
PCB layout complexity	Low	High	Medium
EMI performance (qualitative)	Poor	Good	Excellent
Relative BOM cost	Low	Highest	High

Prices are based on the specific Wolfspeed SiC devices used in the simulations, accounting for required paralleling where applicable to make an equal power rating. While passive components and packaging also influence total system cost, this table captures the relative differences in complexity and active component cost, highlighting the trade-offs between the 2L H-Bridge, 3L ANPC, and 3L T-Type configurations.

5 Conclusion

This paper presented a detailed comparative study of three inverter topologies—2L H-Bridge, 3L ANPC, and 3L T-Type—for high-voltage (post-800V) electric vehicle traction applications. Using discrete SiC MOSFETs, the electro-thermal-oriented and EMI-focused simulations evaluated power losses, junction temperature swings, conducted EMI behavior, efficiency, and active component cost under air natural cooling conditions across input voltages of 800 V, 1000 V, and 1200 V.

The results showed that while the 2L H-Bridge offers structural simplicity and lower device count, it suffers from higher switching losses, elevated junction temperatures, and poor EMI performance due to full DC-link voltage transitions. The 3L ANPC topology improves EMI behavior and switching loss profile due to reduced voltage stress per switching event, but incurs higher conduction losses because of longer current conduction paths. Among the evaluated topologies, the 3L T-Type inverter consistently demonstrated the best overall performance, achieving the highest efficiency, lowest thermal stress, and superior EMI characteristics, making it a strong candidate for next-generation high-voltage EV applications.

Although this study provides important insights into the electro-thermal and EMI trade-offs among different inverter structures, further research is necessary to address additional challenges arising in post-800V systems. In particular, future work should focus on evaluating the long-term reliability of high-voltage traction inverters, where insulation aging, partial discharge effects, and thermal cycling stress become critical factors. Moreover, the development of robust fault detection, protection, and isolation strategies for high-voltage EV systems is essential to ensure safety under abnormal operating conditions. As the EV industry continues advancing toward higher charging speeds, integrating high-voltage traction inverters with evolving fast-charging infrastructure and standardizing safety margins for ultra-high-voltage operation represent important research directions.

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