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Mission Profile based Traction Inverter Design Considerations for Sustainability using Multiphysics Approach

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Executive Summary

As the global push toward carbon neutrality accelerates, the sustainability of power electronics has garnered increasing attention from both academia and industry. However, a standardized methodology for evaluating power electronics sustainability—particularly in the context of traction inverters—remains underdeveloped due to the lack of comprehensive databases and systematic assessment frameworks. This paper, building on Volvo's extensive design experience, introduces an enhanced evaluation methodology for traction inverter sustainability. The proposed approach integrates advanced component modeling techniques using a multi-physics-based framework, enabling a more precise analysis of the environmental impact associated with different power electronics technologies. By incorporating factors such as material selection, thermal performance, reliability, and overall system efficiency, this methodology provides a holistic perspective on sustainability assessment. To illustrate its effectiveness, several case studies are presented, demonstrating the application of this approach to various traction inverter designs. These examples highlight the influence of technological advancements on sustainability metrics, offering valuable insights into optimizing next-generation traction inverters for improved environmental performance.

Keywords: Traction inverter, Multiphysics design, Sustainability, Carbon footprint, Mission profile.

1 Introduction

The global energy crisis is becoming increasingly severe, highlighting the urgent need for sustainable transportation solutions [1]. In this context, electric vehicles (EVs) offer significant advantages over conventional internal combustion engine vehicles, primarily by reducing dependence on fossil fuels and minimizing carbon dioxide (CO_2) emissions. As a critical component of EV powertrains, the traction inverter plays a fundamental role in converting direct current (DC) energy from the battery into alternating current (AC) energy required by the electric machine. The advancement of high-voltage power electronics technology has facilitated extensive research on various traction inverter topologies over the past decades, with a focus on improving efficiency, reliability, and performance [2] – [4]. However, despite substantial technological progress, the sustainability aspect of traction inverters—particularly the evaluation of different power electronics technologies concerning their environmental impact—has received comparatively little attention.

The sustainability of traction inverters is inherently linked to the materials used in their construction. These systems comprise various components, each contributing to the overall environmental footprint. The power semiconductor module, serving as the core functional unit, consists of semiconductor materials, copper, aluminum, and ceramics. Additionally, the DC-link capacitor plays a crucial role in stabilizing voltage and mitigating current ripple, ensuring stable inverter operation. Copper busbars, particularly DC laminated busbars, are essential for establishing electrical connections between the DC-link capacitor and the power semiconductor module. The manufacturing of these power electronics components inevitably leads to greenhouse gas (GHG) emissions, including CO_2, further underscoring the need for sustainability assessment methodologies.

To systematically evaluate the environmental impact of traction inverters, the concept of carbon footprint—originating from the ecological footprint framework proposed by William E. Rees and Mathis Wackernagel at the University of British Columbia in 1990—is employed. Carbon footprint analysis provides a quantitative measure of the total CO_2 emissions associated with the lifecycle of a product, from raw material extraction and component manufacturing to operational efficiency and end-of-life disposal. In this study, a comprehensive carbon footprint model is developed based on a multi-physics modeling approach, considering various mission profiles. The proposed model accounts for the material composition, manufacturing processes, and operational characteristics of traction inverters, providing a holistic perspective on their sustainability.

Using this methodology, different traction inverter architectures are evaluated, including multi-phase topologies [5] and flying capacitor-based configurations [6]. By analyzing the carbon footprint of these architectures, this study aims to provide valuable insights into the environmental impact of various power electronics technologies and guide the development of more sustainable traction inverter designs. The findings contribute to a deeper understanding of sustainability in power electronics, paving the way for future research and innovation in environmentally conscious EV powertrain solutions.

2 Proposed Design Methodology

Figure 1 illustrates the proposed methodology for carbon footprint assessment. The evaluation framework focuses on three key components: the power module, DC-link capacitor, and busbar. Based on the specified mission profile, the selected traction inverter architecture is assessed with respect to these critical components.

The mission profile serves as a primary design input for this evaluation, as it directly influences the sizing of the three main components. For example, the amount of copper required is determined by the level of AC current the system must support. In addition, the traction inverter architecture is another critical factor; the chosen topology significantly affects parameters such as the DC-link capacitor value. In the initial stage of this assessment, only thermal requirements are considered, as they play a pivotal role in determining the dimensions and specifications of key components. For instance, if a lower junction temperature is required, it may necessitate either a more robust heatsink—potentially increasing copper usage in the pin-fin structure—or a higher number of semiconductor dies within the power module.

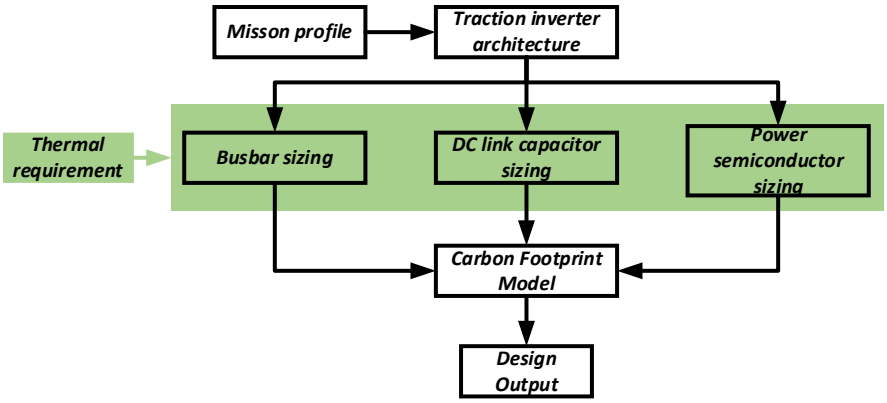

Figure 1: Proposed design methodology.

Once the key component dimensions are defined, a carbon footprint model is employed to assess the environmental impact associated with each component. This model is based on a comprehensive database that quantifies the carbon footprint contributions of various material manufacturing processes. Typically, carbon footprint is calculated based on mass. For instance, busbar carbon footprint is defined as how many kg of **CO_2e** generated if 1 kg copper busbar is manufactured. In the subsequent subsections, the carbon footprint evaluation methodologies for the busbar, DC-link capacitor, and power semiconductor will be individually detailed.

2.1 Copper busbars

Copper is a fundamental material utilized across all three key components. Its required quantity—expressed in kilograms to support the specified AC output current—is determined using the workflow illustrated in Figure 2(a). The mission profile provides critical design inputs, including the output AC current (I_{ORMS}) and total operating time. Additionally, thermal management parameters—such as the cooling method (air or liquid) and the ambient or coolant temperature—are essential considerations. DC busbar will follow a similar process as AC busbar.

In this analysis, the length of the AC busbar is assumed to be constant, while the cross-sectional area is treated as a design variable. This variable is optimized through electro-thermal simulations, as shown in Figure 2(b), to determine the final mass of the busbar. Subsequently, using data from the carbon footprint database, the environmental impact associated with the copper used in the AC busbar is quantified.

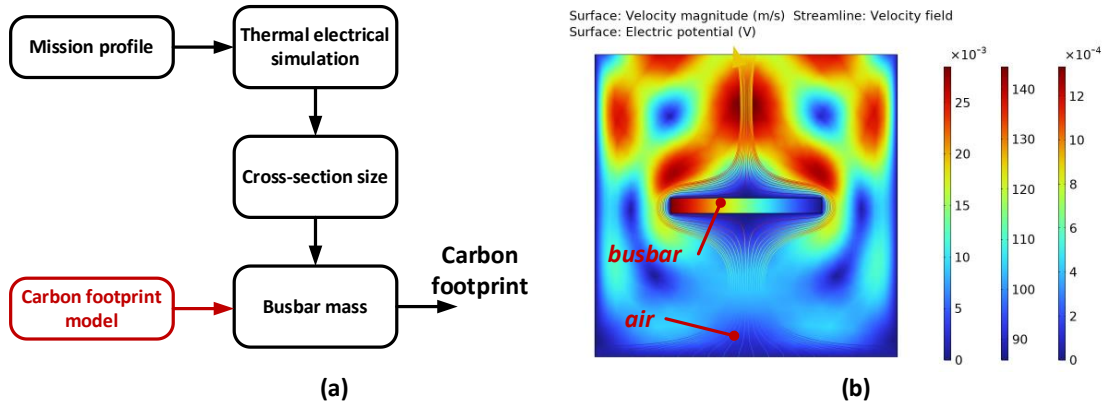

Figure 2: (a). Proposed design methodology for busbar. (b). busbar thermal electrical simulation.

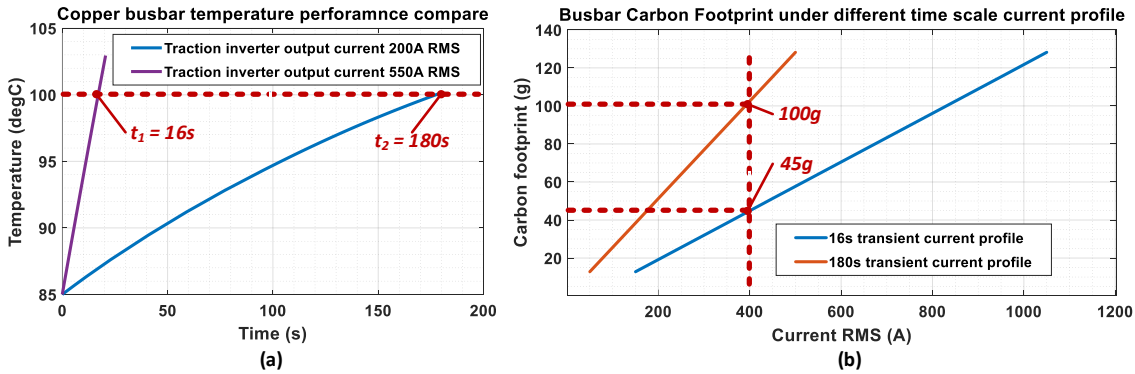

Figure 3: (a) busbar temperature rise under different traction inverter output current. (b). carbon footprint for busbar under different mission profile with different time duration – ***16s and 180s with fixed 400 A output current***.

Figure 3(a) illustrates the thermal performance of a fixed-size (or fixed-mass) busbar under different traction inverter mission profiles. The blue curve represents the temperature rise of the busbar when subjected to a mission profile of 180 seconds at 200 Arms output current. As shown, the busbar temperature reaches 100 °C within 180 seconds, based on a comprehensive Multiphysics simulation

incorporating electrical, electromagnetic, and thermal effects, as illustrated in Figure 2(b).

Under the same temperature rise constraint, if the output current is increased to 550 Arms, the busbar reaches 100 °C in just 16 seconds. Therefore, for a mission profile requiring 550 Arms over 180 seconds, the busbar size must be increased—assuming the cooling system remains unchanged—to limit the temperature rise within acceptable limits. This analysis clearly demonstrates that the mission profile has a significant impact on busbar sizing.

Figure 3(b) presents the corresponding carbon footprint of busbars under two mission profiles: 16 s / 400 Arms and 180 s / 400 Arms. According to the simulation results in Figure 3(a), sustaining 400 Arms for 180 seconds results in a busbar carbon footprint - CO_2-equivalent (**CO_2e**) of 100 grams. In contrast, when the duration is reduced to 16 seconds, the **CO_2e** drops to 45 grams. These results underscore that the mission profile is a critical design input and must be considered when assessing the sustainability of traction inverter components.

2.2 DC link capacitor

Figure 4 illustrates the proposed methodology for evaluating the carbon footprint of the DC-link capacitor. This process requires four key inputs: the mission profile, traction inverter topology, stray inductance requirements, and cooling conditions. Mission profile and inverter topology determine the required DC-link capacitance and the associated ripple current. Both the ripple current and stray inductance specifications influence the design of the internal copper busbars within the DC-link capacitor package, primarily from an electromagnetic performance standpoint.

In parallel, thermal analysis introduces additional constraints on the internal busbar configuration. Specifically, the temperature requirements of the capacitor cells may necessitate adjustments not only to the busbar design but also to the choice of packaging materials, as illustrated in Figure 5. Together, these electrical, electromagnetic, and thermal considerations form the basis for assessing the carbon footprint of the DC-link capacitor.

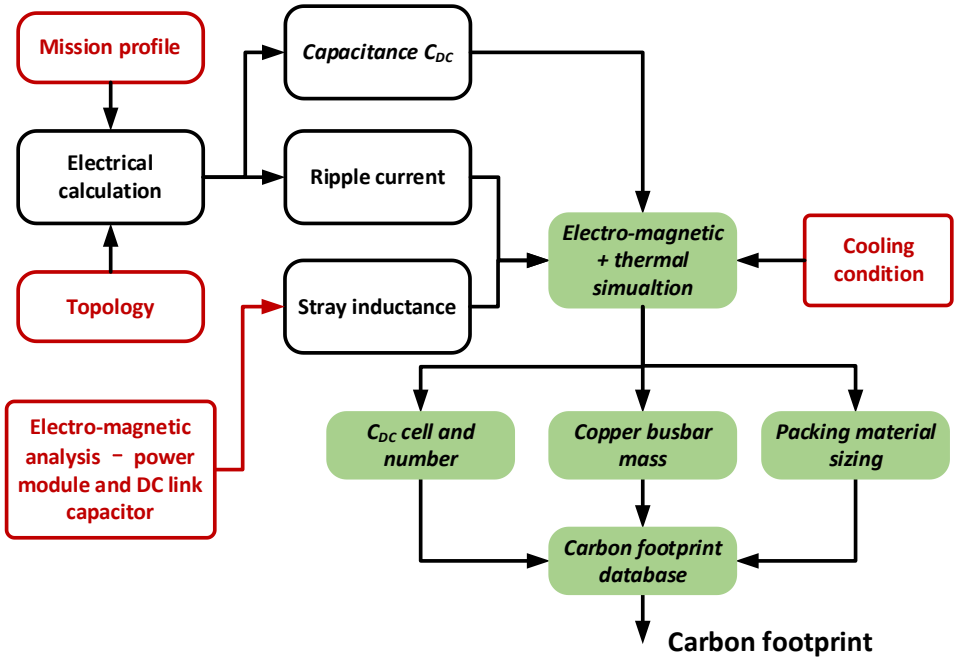

Figure 4: Proposed design methodology for DC link capacitor

Figure 5 presents the results of electro-thermal simulations conducted under various design scenarios while using three phase two level topology. A DC link capacitor composed of four film capacitor cells is configured to achieve a total capacitance of 280 µF with a stray inductance of 15 nH. The baseline design employs a 0.25 mm-thick copper busbar, as shown in Figure 5(a). Under a ripple current of 200 Arms, the

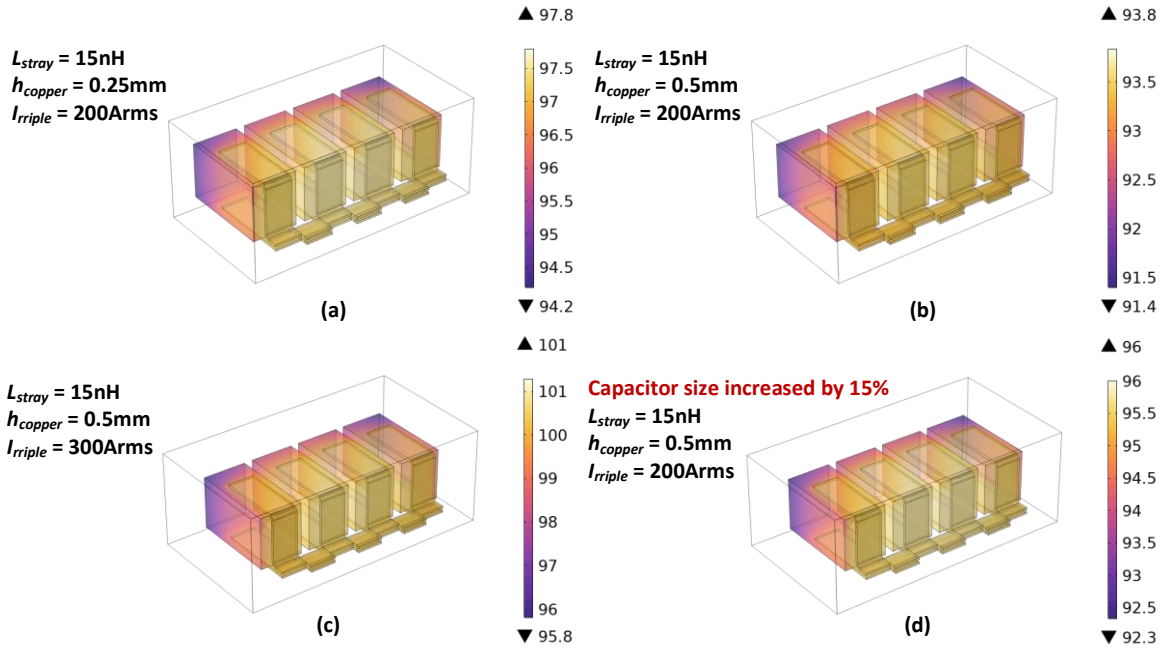

Figure 5: DC link capacitor thermal simulation under different evaluation cases. (a). thin copper busbar inside. (b). thick copper busbar inside. (c). higher rippler current. (d). bigger package size

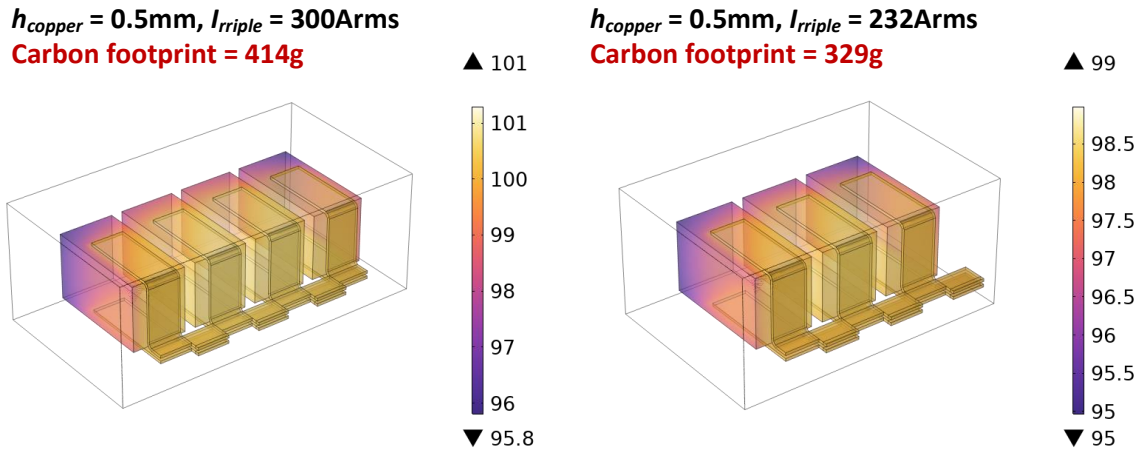

Figure 6: Carbon footprint under different ripple current. (a). I_{ripple} = 300Arms. (b). I_{ripple} = 232Arms.

peak internal temperature reaches 97.8 °C. By increasing the busbar thickness, the thermal hotspot is reduced to 93.8 °C, as illustrated in Figure 5(b). However, this improvement in thermal performance comes at the expense of increased copper usage, which contributes to a higher **CO_2e**.

In Figure 5(c), the impact of an elevated ripple current (300 Arms) on thermal behavior is assessed. The increased current leads to greater ohmic losses not only in the copper busbar but also within the capacitor cells themselves. Consequently, the peak temperature rises to 101.0 °C. To mitigate this, a larger package is implemented—primarily by incorporating more epoxy resin—resulting in a 15% increase in volume. Nevertheless, the peak temperature in this modified configuration is still 96.0 °C, which is only 2.2 °C lower than the high-current case with the smaller package. This suggests that a larger physical package may adversely affect the thermal performance of the DC link capacitor due to increased thermal resistance or reduced cooling effectiveness.

Figure 6 compares two design strategies for achieving a 280 µF DC link capacitor: one utilizing four capacitor cells and the other using three. Despite providing the same total capacitance, these configurations exhibit different capabilities in handling ripple current. From a thermal management perspective, all designs are constrained by the requirement that the maximum temperature must remain

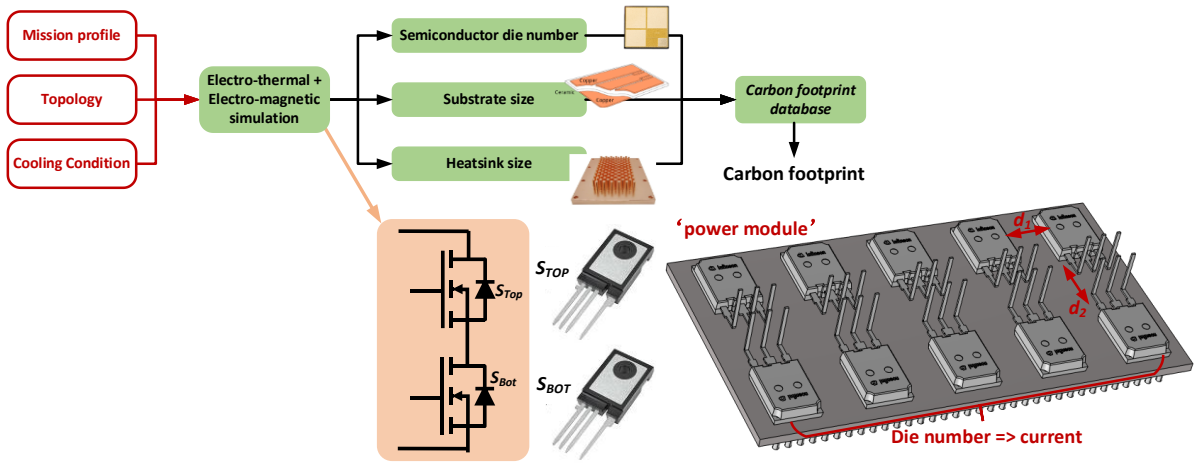

Figure 7: Proposed design methodology for power module

below 100 °C. The design shown in Figure 6(a) supports up to 300 Arms ripple current with an associated carbon footprint of 414 g **CO_2e**, whereas the design in Figure 6(b) accommodates only 232 Arms but has a lower carbon footprint of 329 g **CO_2e**. This illustrates the inherent trade-off between thermal capability and environmental impact in DC link capacitor design.

2.3 Power semiconductor

The power semiconductor module is evaluated based on a half-bridge configuration, which serves as the fundamental building block for most traction inverter topologies, such as the three-phase inverter, as shown in Figure. 7. The mission profile, inverter topology, and cooling conditions collectively influence the thermal behavior of the power module, particularly with respect to the allowable junction temperature—commonly limited to 175 °C for Silicon carbide (SiC) device. In this evaluation, three primary components are considered: the semiconductor dies, the substrate, and the heatsink. These elements are key contributors to both thermal performance and material-related carbon footprint.

Additional critical components within the power module include interconnections and power terminals. The evaluation of power terminals follows a similar approach to that of AC busbars, with the added requirement of meeting stray inductance constraints. Interconnections, however, present a more complex challenge, as they vary significantly across different manufacturers and technologies, making it difficult to generalize their carbon footprint within a standardized evaluation framework.

Hereby, TO247 is used to form different topology by paralleling switch. Inter-connection will be represented the PCB that is used to achieve connection of parallel TO247. $\boldsymbol{d_1}$ and $\boldsymbol{d_2}$ shown in Figure 7 will not only affect the stray inductance $\boldsymbol{L_{stray}}$ for different switches but also determine the thermal coupling between switches, which will affect the thermal resistance $\boldsymbol{R_{TH}}$. The mechanism to find the proper $\boldsymbol{d_1}$ and $\boldsymbol{d_2}$ will follow **[7]**.

Figure 8 shows the carbon footprint comparison for three different mission profiles (same output current $\boldsymbol{I_{ORMS}}$ with different operating time requirement) listed in Table I considering three phase two level-based traction inverter by using two E3M0016120k in parallel considering junction temperature limit <150degC.

Based on Table I, it is observed that for varying mission profiles with different maximum required operating durations $\boldsymbol{T_{operating\_max}}$, ranging from 2 s to 20 s, the heatsink size is correspondingly adjusted to achieve an optimal trade-off among thermal resistance, thermal capacitance, and cost. A smaller heatsink typically exhibits lower thermal capacitance, leading to a more rapid rise in the junction temperature of SiC devices. Consequently, such a design is unsuitable for applications with larger $\boldsymbol{T_{operating\_max}}$. For instance, in the case of $\boldsymbol{I_{ORMS}}$=200Arms and $\boldsymbol{T_{operating\_max}}$=2 s, a relatively compact heatsink is employed due to a smaller spacing parameter $\boldsymbol{d_1}$, resulting in reduced thermal capacitance. However, the smaller $\boldsymbol{d_1}$ also enhances thermal coupling among parallel devices, thereby increasing the overall thermal resistance. As a result, the junction temperature rises more rapidly compared to the other three scenarios. When $\boldsymbol{T_{operating\_max}}$ =5 s, the thermal management capability becomes insufficient to maintain $\boldsymbol{T_{JSiC}}$<150degC. To

Table I: Evaluation details for four mission profile

V_{DC} = 800V	Parallel	d_1 (mm)	d_2 (mm)	Heatsink W*L (mm)
I_{ORMS} = 200Arms $T_{operating\_max}$ = 2s	2	5	20	67*92
I_{ORMS} = 200Arms $T_{operating\_max}$ = 5s	2	15	20	77*92
I_{ORMS} = 200Arms $T_{operating\_max}$ = 10s	2	20	20	82*92
I_{ORMS} = 200Arms $T_{operating\_max}$ = 20s	2	20	20	82*92

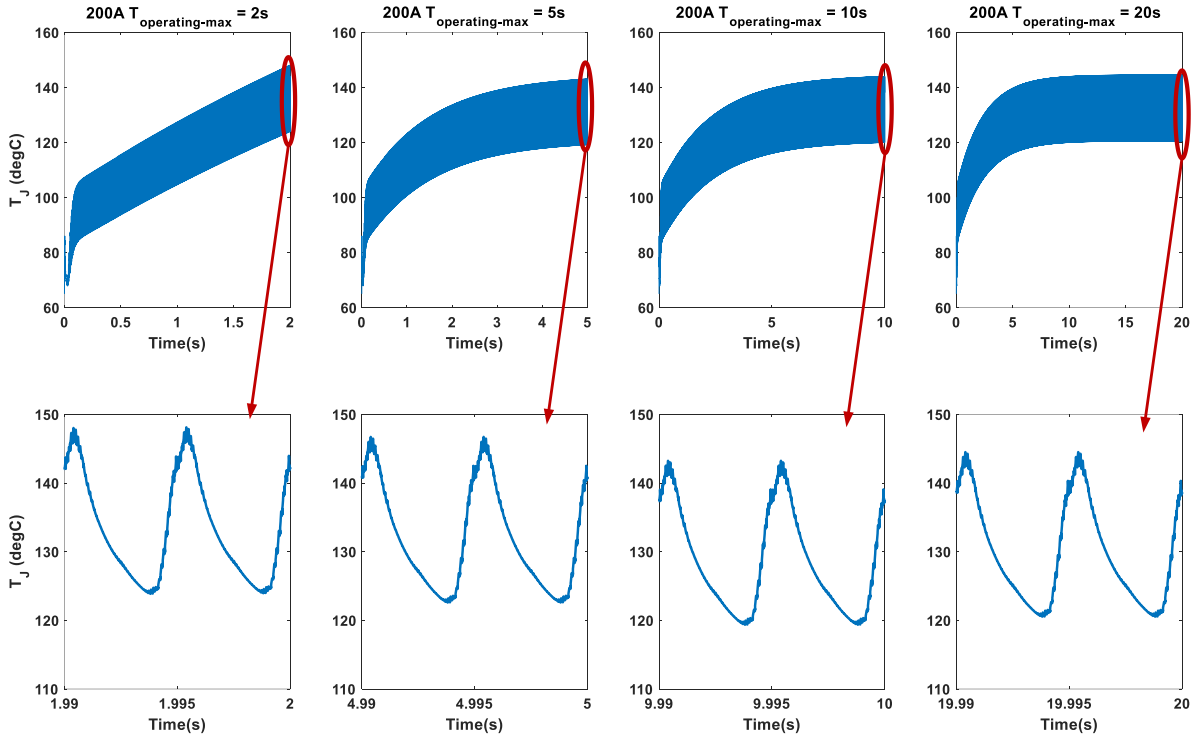

Figure 8: Junction temperature of SiC (T_{JSiC}) with four mission profiles in Table I with 10L/min & 65degC coolant.

address this, a larger spacing of d_1=15 mm is adopted to improve thermal capacitance, allowing a slower junction temperature rise and mitigating thermal coupling effects, which collectively contribute to a lower effective thermal resistance.

For both $T_{operating\_max}$=2s and 5s, the junction temperature of the SiC devices (T_{JSiC}) remains in the transient thermal regime and does not reach a steady-state condition. However, when $T_{operating\_max}$ is extended to 10 s and 20 s, T_{JSiC} begins to approach steady state, as the operating duration exceeds the system's thermal time constant, which is determined by the interplay of thermal capacitance and thermal resistance. If T_{JSiC} remains within the transient region, a significantly larger heatsink is required to manage the thermal load, which compromises both cost-efficiency and power density targets.

Since the number of parallel-connected devices remains constant across the mission profiles presented in Table I, the carbon footprint attributed to the power semiconductors is identical in all cases. However, the carbon footprint associated with the heatsink varies, as illustrated in Figure 9. As $T_{operating\_max}$ increases, the corresponding **CO_2e** emissions also rise. In particular, when $T_{operating\_max}$ reaches 20 s, a trade-off becomes necessary between cost, power density, and the thermal design parameters (i.e., thermal resistance and capacitance). To mitigate thermal coupling effects under this longer operating duration, the spacing d_1 between parallel devices, as shown in Figure 7, is increased. This design choice reduces thermal interaction but also leads to a higher **CO_2e** footprint due to the additional copper material required.

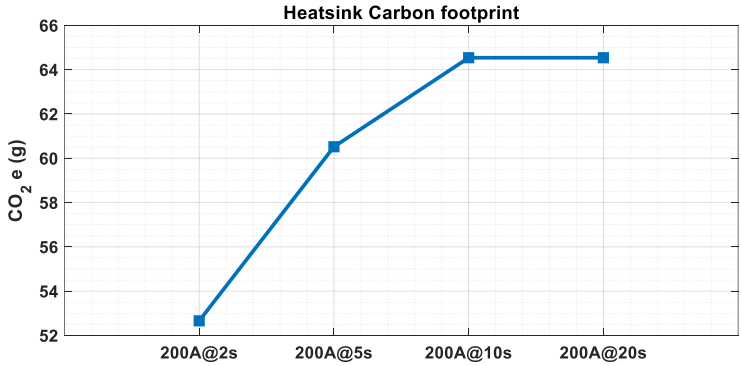

Figure 9: Heatsink carbon footprint under four different mission profile.

3 Analysis Examples

The methodology outlined in Section 2 has been applied to evaluate the impact of different traction inverter topologies on carbon footprint, as illustrated in Figure 10. The topologies under consideration include the conventional three-phase two-level inverter, the flying-capacitor inverter, and the six-phase two-level inverter. In Figure 10, the red lines represent the internal busbar connections within the traction inverter, the green lines denote capacitor components, and the black segments correspond to the power semiconductor modules. The operational conditions for the traction inverter configurations are summarized in Table II.

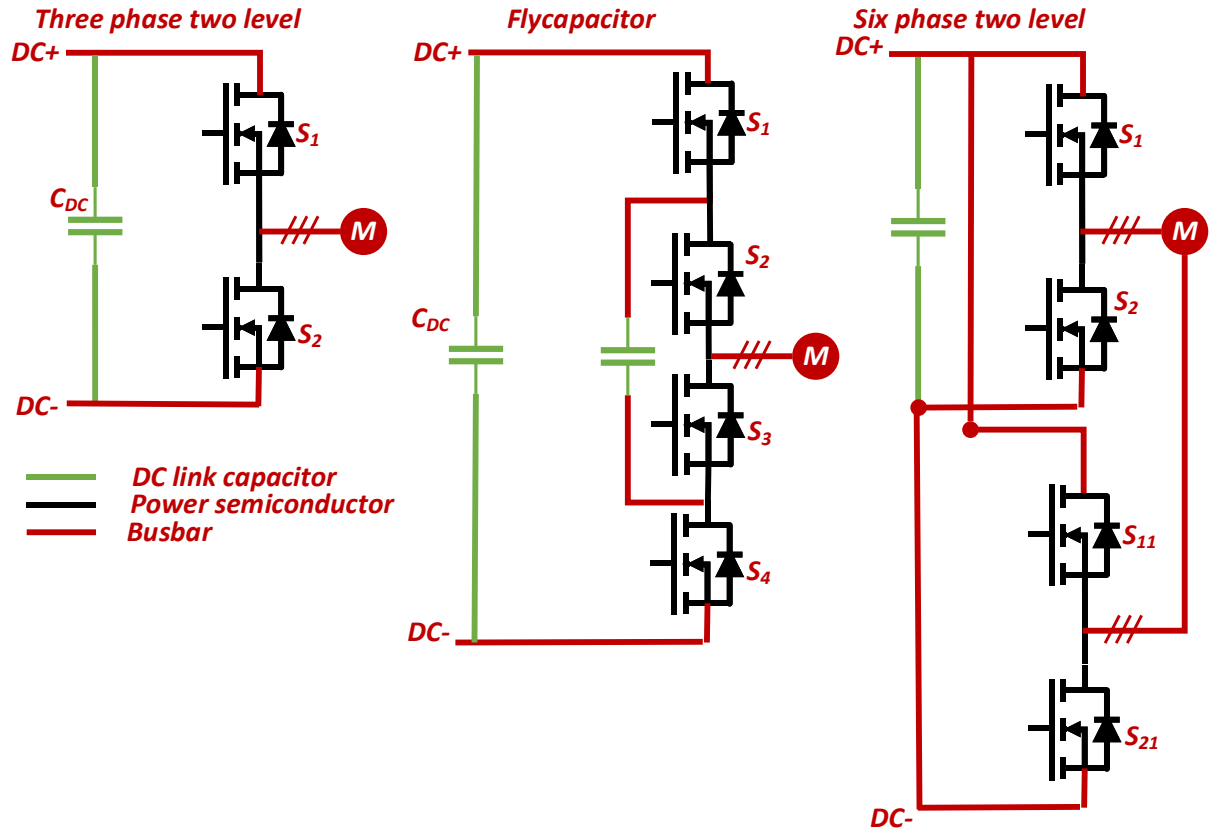

Figure 10: three traction inverter topology – three phase two level, fly-capacitor and multi-phase – 6 phase.

Table II: Design information

	VDC (V)	AC Current (Arms)	T_{hot} capacitor	T_{hot} busbar	T_J power semiconductor
Requirement	800	200 @1min	<100degC	<110degC	<150degC

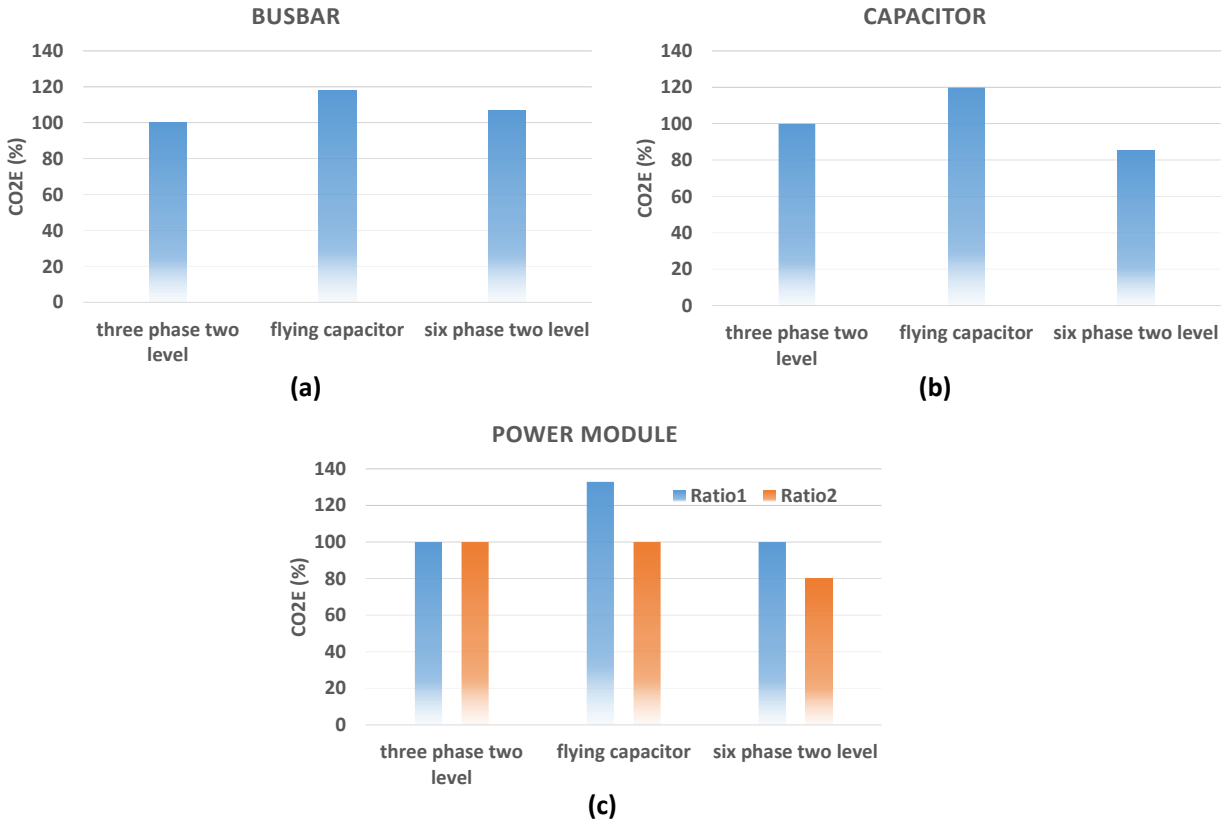

Figure 11: CO2e comparison considering busbar, DC link capacitor and power module.

Figure 11(a) and (b) present a comparative analysis of the **CO_2e** emissions associated with the busbars and DC-link capacitors for different inverter topologies. The conventional three-phase two-level inverter is used as the reference baseline (normalized to 100%). The flying-capacitor topology exhibits a significantly higher **CO_2e** contribution from both busbars and DC-link capacitors, primarily due to the inclusion of additional flying capacitors. The six-phase two-level inverter shows a slightly increased **CO_2e** from the busbar components compared to the three-phase topology, but it offers a lower **CO_2e** for the DC-link capacitor, outperforming the other two configurations in this aspect.

Regarding the power semiconductor modules, two estimation scenarios are illustrated in Figure 11(c). Since specific **CO_2e** data for power module manufacturing is currently not publicly available, the evaluation relies on the energy consumption required for fabricating SiC dies. The types of SiC devices utilized in each topology are listed in Table III. In terms of voltage rating, the energy consumption for manufacturing a 1.2 kV SiC die is estimated to be approximately 1.5–2 times that of a 650 V die. For current rating, a 125 A SiC die requires roughly 1.6–2.5 times the energy of a 70 A counterpart. Accordingly, two scenarios are considered: **Ratio 1** assumes a factor of 1.5 for voltage and 1.6 for current, while **Ratio 2** assumes 2.0 and 2.5, respectively.

Under **Ratio 1**, the flying-capacitor inverter demonstrates the highest **CO_2e** among the three topologies, whereas the six-phase and three-phase two-level inverters yield comparable **CO_2e** levels. In contrast, for **Ratio 2**, the six-phase two-level topology achieves the lowest **CO_2e**, while the three-phase and flying-capacitor topologies exhibit similar and comparatively higher **CO_2e** values.

Table III: Device votlage and current ratings for three topologies.

	Three phase two level	Flying capacitor	Six phase two level
Device Voltage	1.2kV	650V	1.2kV
Device Current (25degC)	125A	125A	70A

4 Conclusion

This paper presents a multi-physics-based methodology for evaluating the sustainability of key components within traction inverters, including power semiconductors, busbars, and DC-link capacitors. The mission profile is incorporated as a critical input parameter, given its substantial influence on the design and thermal management of these components, such as accelerating, high speed low torque, which could result in over design. The proposed evaluation framework is applied to assess the carbon footprint (expressed in **CO_2e**) of three inverter topologies: the conventional three-phase two-level inverter, the flying-capacitor inverter, and the six-phase two-level inverter. The results indicate that the flying-capacitor topology exhibits a significantly higher **CO_2e** associated with both the DC-link capacitor and busbar subsystems, primarily due to the inclusion of additional passive components. Regarding power modules, the energy consumption associated with manufacturing semiconductor dies is used as a representative metric for **CO_2e** emissions. Establishing a publicly accessible database for **CO_2e** values would significantly enhance the accuracy and reliability of environmental impact assessments.

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Presenter Biography

Chi Zhang (Senior Member, IEEE) received the B.Eng. degree in electronics and information engineering in 2012, the Master degree in Power electronics and electrical drive in Zhejiang University, Hangzhou, China, in 2013 and the Ph. D degree in Energy Technology (Power Electronics and Drives) from Aalborg University, Aalborg, Denmark, in 2016.
He started to lead automotive traction inverter design in Inovance, China. In 2019, he joined Raytheon Technologies as a senior research scientists, where he is responsible for wind band gap power device package and converter design. And he received Outstanding Achievements Award due to his contribution for Mega-Watt Motor Controller for Electrified Aircraft. He is now worked as senior engineer in Volvo cars since 2022. His research area includes multi-physics based power converter design and optimization, power semiconductor device package, reliability and gate driver design. He is the holder of 3 USA patents, more than 10 European patents (in process) and 8 Chinese patents.